REMARKS

In response to the Advisory Action mailed August 27, 2004, Applicant respectfully requests reconsideration. To further the prosecution of this Application, Applicant submits the following remarks, has canceled claims and has added new claims. The claims, as presented, are believed to be in allowable condition.

Claims 1-42 were pending in this Application. Claims 30-31 and 41-42 have been canceled without prejudice as to the subject matter recited therein. Applicant expressly reserves the right to prosecute the canceled claims and similar claims in one or more related Applications. Claims 43-48 have been added. Accordingly, claims 1-29, 32-40 and 43-48 are now pending in this Application. Claims 1, 11 and 21 are independent claims.

Rejection under §102

Claims 1-29 and 32-40 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,425,034 (Steinmetz et al.). Applicant respectfully submits that the claims, as amended, patentably distinguish over the cited prior art.

Steinmetz discloses a host system 180 having a host bus adaptor 182 which connects to a number of peripheral devices 186 through a high-speed serial FC data stream 188 (column 8, lines 45-54 and Figs. 4 and 5). The host bus adaptor 182 utilizes a fibre channel controller 190 (column 8, lines 55-58). Steinmetz further discloses a disk array controller 200 which uses the fibre channel controller 190 (column 8, lines 64-65 and Figs. 5 and 6). For example, the disk array controller 200 includes a cache memory 210 which connects to an FC controller 206 through a PCI bus 208, and connects to other FC controllers 216A-216N through another PCI bus 214 to interface to a mass storage system 204 (column 9, lines 1-8 and Fig. 6).

Claims 1-10 and 32-35

Claim 1 is directed to a method which is performed in an interface circuit of a data storage system. A point-to-point channel directly connects to both the interface circuit and a volatile memory cache circuit. The method involves exchanging data with the volatile memory cache circuit. The method includes the steps of providing a command to the volatile memory cache circuit through the point-to-point channel which directly connects to both the interface circuit and the volatile memory cache circuit, moving a data element through the point-to-point channel in accordance with the command, and receiving status from the volatile memory cache circuit through the point-to-point channel in accordance with the data element.

The cited prior art does not teach a method for exchanging data with a volatile memory cache circuit which has a step of providing a command to the volatile memory cache circuit through a point-to-point channel which directly connects to both an interface circuit and the volatile memory cache circuit, as recited in claim 1. Rather, Steinmetz discloses an FC controller 206 which communicates with a cache memory 210 through a multi-drop PCI bus 208 that directly connects to the cache memory 210 (e.g., see column 8, lines 49-52; column 9, lines 1-4 and Fig. 6 of Steinmetz).

For the reasons stated above, claim 1 patentably distinguishes over the cited prior art, and the rejection of claim 1 under 35 U.S.C. §102(e) should be withdrawn. Accordingly, claim 1 is in allowable condition.

Because claims 2-10 and 32-35 depend from and further limit claim 1, claims 2-10 and 32-35 patentably distinguish over the cited prior art for at least the same reasons.

Claims 11-20 and 36-38

Claim 11 is directed to a method which is performed in a volatile memory cache circuit of a data storage system. A point-to-point channel directly connects to both an interface circuit and the volatile memory cache circuit. The method

involves exchanging data with the interface circuit. The method includes the steps of receiving a command from the interface circuit through the point-to-point channel which directly connects to both the interface circuit and the volatile memory cache circuit, moving a data element through the point-to-point channel in accordance with the command, and providing status to the interface circuit through the point-to-point channel in accordance with the data element.

The cited prior art does not teach a method for exchanging data with a volatile memory cache circuit which has a step of receiving a command from an interface circuit through the point-to-point channel which directly connects to both the interface circuit and the volatile memory cache circuit, as recited in claim 11. Rather, as explained above in connection with claim 1, Steinmetz discloses an FC controller 206 which communicates with a cache memory 210 through a multi-drop PCI bus 208 that directly connects to the cache memory 210 (e.g., see column 8, lines 49-52; column 9, lines 1-4 and Fig. 6 of Steinmetz). Accordingly, claim 11 patentably distinguishes over the cited prior art for at least the same reasons as claim 1, and the rejection of claim 11 under 35 U.S.C. §102(e) should be withdrawn. As a result, claim 11 is in allowable condition.

Because claims 12-20 and 36-38 depend from and further limit claim 11, claims 12-20 and 36-38 patentably distinguish over the cited prior art for at least the same reasons.

Claims 21-29 and 39-40

Claim 21 is directed to a data storage system which includes a volatile memory cache circuit that buffers data elements exchanged between a storage device and a host, and an interface circuit that operates as an interface between the volatile memory cache circuit and at least one of the storage device and the host. The data storage system further includes a point-to-point channel interconnected between the volatile memory cache circuit to the interface circuit. The point-to-point channel carries the data elements between the volatile

memory cache circuit and the interface circuit. The point-to-point channel directly connects to both the interface circuit and the volatile memory cache circuit.

The cited prior art does not teach a data storage system having a point-to-point channel point-to-point channel directly connecting to both an interface circuit and a volatile memory cache circuit, as recited in claim 21. Rather, as explained above in connection with claim 1, Steinmetz discloses an FC controller 206 which communicates with a cache memory 210 through a multi-drop PCI bus 208 that directly connects to the cache memory 210 (e.g., see column 8, lines 49-52; column 9, lines 1-4 and Fig. 6 of Steinmetz). Accordingly, claim 21 patentably distinguishes over the cited prior art for at least the same reasons as claim 1, and the rejection of claim 21 under 35 U.S.C. §102(e) should be withdrawn. Thus, claim 21 is in allowable condition.

Because claims 22-29 and 39-40 depend from and further limit claim 21, claims 22-29 and 39-40 patentably distinguish over the cited prior art for at least the same reasons.

Newly Added Claims

Claims 43-48 are newly added and are believed to be in allowable condition. Claims 43-44 depend from and further limit claim 1. Claims 45-46 depend from and further limit claim 11. Claims 47-48 depend from and further limit claim 21. Support for claims 43-48 is provided in the Specification, for example, on pages 8, line 15 through page 9, line 29 and in Fig. 2. No new matter has been added.

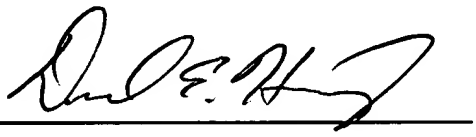
Conclusion

In view of the foregoing remarks, this Application should be in condition for allowance. A Notice to this affect is respectfully requested. If the Examiner believes, after this Amendment, that the Application is not in condition for allowance, the Examiner is respectfully requested to call the Applicant's Representative at the number below.

Applicant hereby petitions for any extension of time which is required to maintain the pendency of this case. If there is a fee occasioned by this Amendment, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 50-0901.

If the enclosed papers or fees are considered incomplete, the Patent Office is respectfully requested to contact the undersigned collect at (508) 366-9600, in Westborough, Massachusetts.

Respectfully submitted,



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